

## Yuehao Hu

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## Education

MSc | Computer Science | Simon Fraser University

2024 – Present

BEng | Internet of Things (IoT) Engineering | Chengdu University of Technology

2011 - 2015

## Publications

FARLock: Asymmetric RDMA Locking Made Fair. (to appear)

Yuehao Hu, Jiatang Zhou, Tianzheng Wang and Keval Vora.

OSDI 2026

## Work Experience

Graduate Research Assistant | Advised by Dr. Keval Vora | SFU

Sep 2024 - Present

- Conduct research on disaggregated memory, focusing on **RDMA**-based synchronization techniques.
- Designed and implemented FARLock, a distributed asymmetric locking mechanism, significantly improving system fairness and reducing tail latencies under high contention, applicable to time-sensitive applications in cloud data centers.
- Developed a scalable **C++** benchmarking framework, paired with **Python** deployment scripts, to rigorously evaluate diverse **RDMA**-based locking mechanisms across multi-node clusters.
- Integrated the custom locking mechanism into **Sherman** (an RDMA-based distributed indexing system), improving query tail latency by up to 14x.

Distributed Storage Development Engineer | Enmotech

Mar 2021 – Jan 2024

- Contributed to the development of zStorage, a distributed storage system optimized for database workloads, deployed via zDataX (Enmotech's database appliance) across healthcare, cloud data center, and finance industries.
- Designed and implemented **Raft**-based consensus for the chunk server (**C/SPDK, RDMA**), enabling reliable data replication, dynamic membership changes, and automated failure recovery.
- Developed management plane features utilizing **Go, Gin, and RESTful APIs** to facilitate capacity balancing, QoS policies, and scalable, containerized multi-architecture deployments.

Software Engineer | Chengdu Xingduowei Technology

Jan 2020 – Feb 2021

- Developed firmware for industrial motion controllers used in CNC systems (**C, STM32, Keil**).
- Led the design and implementation of motion planning algorithms, including linear and S-curve acceleration profiles and velocity lookahead optimization.
- Redesigned the CAD file processing algorithm in the host-side control software (**C++, Qt**), reducing processing time for large files by up to 300x.

Software Engineer | Alpha Networks

Mar 2017 - Jun 2019

- Developed and maintained firmware for state-of-the-art Ethernet switches (**C, VxWorks**), contributing to core networking features and system stability.
- Designed and implemented the PD-Alive feature, enabling switches to monitor the health of connected Power over Ethernet (PoE) devices via **ICMP/ICMPv6** probing and traffic monitoring; implemented a lightweight **ARP/ICMP** mechanism bypassing the network stack to overcome session limits.
- Implemented hardware drivers on **VxWorks RTOS** for multiple subsystems, including physical-layer (PHY) interfaces, PoE controllers, and flash storage.

## Skills

Languages: C/C++, Go, Python, Java, C# | Systems & Infrastructure: Linux, VxWorks, RDMA, SPDK, MPI, Raft

Tools: Git, SVN, Jenkins, Docker, Qt, Keil